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Overview of Capacitive Couplings in Windings

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***Abstract*—The use of electrical machines (EMs) with variable-frequency drives (VFDs) results in electromagnetic interference (EMI). At high frequencies (HFs) of conducted EMI, the impedance of an EM insulation system fed from a VFD is small due to the parasitic capacitive couplings. Thus, the conducted EMI currents flow through the insulation into the other conductive parts of the machine or ground. This can cause damage to the insulation, accelerate corrosion and bearings, and influence other electrically and/or mechanically connected equipment in the system. In order to understand the phenomena of EMI and how to minimize it, one must understand parasitic capacitances in a VFD-cable-EM system. Many authors analyze the topic of parasitic capacitances of cables and machine's bearing capacitances. However, not many publications are focused on the detailed analysis of the windings. In most cases, the parasitic capacitances of the winding are represented as a part of a global equivalent RLC circuit. Some authors use simplified models such as solenoids, which are not adequate representatives of the actual winding topologies used in EMs. To date, not much attention is given to the actual distribution of parasitic capacitive couplings in the winding itself, especially for multi-layer coils. Therefore, it appears necessary to provide an overview of the models proposed in the literature and their implementation in the analysis of EMs. This paper presents capacitive couplings from the point of view of winding topology and conductor geometry, including insulation coating between conductors, and conductor and ground, which can be implemented in the winding equivalent RLC circuit, which can further be applied to analyze the machine's behavior at HFs. The discussion section at the end of this paper recommends further steps on how to determine the parasitic capacitive couplings in the future with more accuracy.**

Keywords*—*electric machines; windings; coils; insulation system; capacitance; capacitive coupling; electromagnetic interference; variable-frequency drive.

I. INTRODUCTION

Electrical machines in combination with variable-frequency drives are widely present in almost any application today [1-3]. Some advantages of using VFDs are: higher efficiency of a driven motor, fast control response, accurate speed control, good torque response, etc. [4, 5]. High switching frequency of VFD in correlation with the high rate of voltage rise and fall times (50-300ns [6-9]), sets a significant voltage stress on the winding insulation system. Winding insulation system, together with two conductive parts of the machine, forms a capacitive coupling. Inside an EM, the following capacitive couplings can be observed, as shown in Fig. 1 [10]:

- stator winding-to-core capacitance (C_{WS});
- phase-to-phase capacitance (C_{PP});
- stator winding -to-rotor capacitance (C_{WR});
- stator core-to- rotor capacitance (C_{SR});
- bearing capacitance (C_{BI} and C_{BO}).

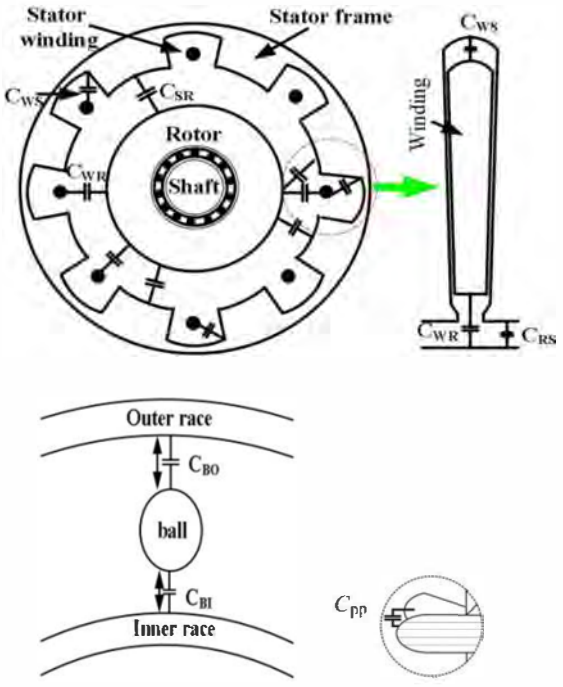

Fig. 1. Capacitive couplings inside an EM [10]

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At low frequencies, mentioned capacitive couplings can be neglected, considering their very low value (i.e. order of tenths of pF [11] up to tenths of nF [12, 13]). However, the effect of these couplings becomes apparent in inverter-driven EM due to the high frequency (HF) switched voltages. The resulting effects are conducted and radiated electromagnetic interference (EMI). The radiated EMI, found in the 30MHz-40GHz frequency range, will not be addressed in this paper [14]. The conducted EMI, however, is manifested through differential- and common-mode voltages and currents (DMV, DMC, CMV and CMC, respectively) with harmonic frequencies ranging from 150kHz up to 30MHz [15-17]. Electronic switching elements inside an inverter, i.e. IGBTs, represent the source of this unwanted EMI. The differential-mode noise is also referred as symmetrical noise or line-to-line noise. DMC flows through one phase and returns through the other (line-to-line path). Common-mode noise is referred as asymmetrical noise or line-to-ground noise. CMC flows through all phase conductors and returns via the ground conductor. Differential- and common-mode paths are presented in Fig. 2. Connections between the phase conductors and the ground conductor are realized via (parasitic) capacitive couplings between the phase windings and the ground (i.e. stator and/or rotor core).

Unlike grid supplied machines, pulse-width modulation (PWM) inverter-fed machines inherently result in CMV on the connection point of the machine phase windings, which has a value at any point in the time as shown in the example given in Fig. 3 [18-20]. In Fig. 3a reference voltage signals are presented with red, green and blue sinusoidal signals, while triangle carrier signal is marked black. In diagrams in Figs. 3b-3d, red, green and blue rectangular signals, respectively, represent output signals of the inverter. These are also signals at the machine's input. The diagram in Fig. 3e presents the CMV signal at the machine's neutral point in respect to ground. The frequency of CMV is three times higher than the switching frequency of the inverter's IGBTs [21, 22].

Above mentioned parasitic effects can cause premature failure of the electrical insulation and bearings [23, 24]. Further, equipment connected to the EM shaft (e.g. gearboxes, cooling systems) can be affected by shaft-to-ground capacitive currents, possibly leading to damage. To

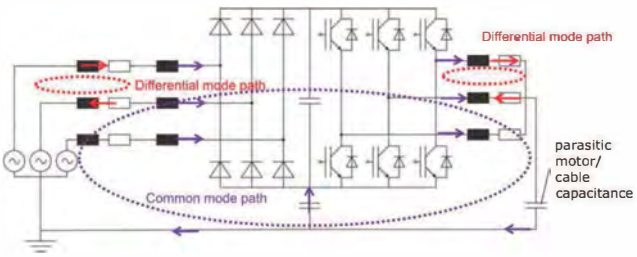

Fig. 2: Differential and common mode paths in VFD

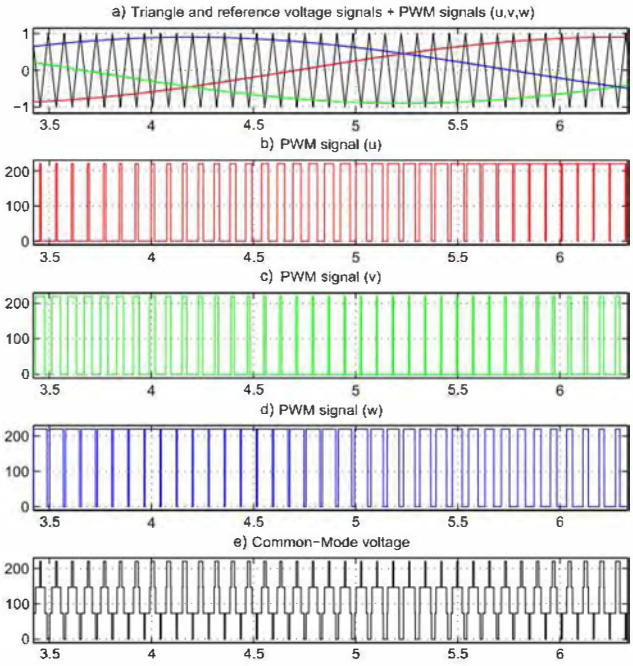

Fig. 3: PWM signals; a) sinusoidal reference voltage signals and the carrier signal; b) PWM signal of first phase; c) PWM signal of second phase; d) PWM signal of third phase; e) CMV signal at the neutral point in reference to the ground [20]

prevent mentioned damage, one must minimize the capacitive couplings. However, in order to analyze parasitic capacitive couplings at HFs, equivalent circuit of a winding and a coil at HF as in Section 3 must be observed [25-32]. This paper presents an overview of the most common and applied analytical methods for calculation of the parasitic capacitances of different types of windings which are given in Section 4 [25-46]. Parasitic capacitive couplings in the bearings and between stator and rotor core will not be addressed in this paper.

II. WHY MINIMIZING THE CAPACITIVE COUPLING?

For EMs, which are working with 50Hz or 60Hz nominal frequency, the insulation system of the windings is usually designed according to the EM manufacturer's best practice and experience and based on general standards and latest technologies. Even for inverter-fed EM with nominal frequency e.g. 400Hz, the insulation system will often be the same as for 50/60Hz or enhanced by applying different insulating material of more insulation layers. In order to demonstrate the necessity of minimizing the capacitive couplings of the insulation system, an example given in table 1 shows what happens with the capacitive reactance of the insulation in the case of different frequencies. For this example assumed capacitance of the winding insulation system is 5nF and 5pF.

TABLE 1: EXAMPLE OF INSULATION CAPACITIVE REACTANCE AT DIFFERENT FREQUENCIES

f [Hz]		50	400	150k	30M
$X_C = \frac{1}{\omega \cdot C}$ [Ω]	C=5nF	636.6k	79.6k	212.2	1.1
	C=5pF	636.6M	79.6M	212.2k	1.1k

From this example it can be seen that at 50Hz and even at 400Hz the reactance is still high. However, considering the HF harmonics of CM signals, it is obvious that reactance is almost negligible. It should be noted that this example is only given for the capacitive reactance, while in reality, the total impedance of the winding insulation system should be considered. This impedance can be calculated using the equivalent circuits given in Section 3 or measured with appropriate high current RLC meters.

III. HIGH-FREQUENCY MODEL OF THE WINDING

Referenced publications propose lumped parameter circuit models in order to qualify and quantify parasitic capacitances of windings. To analyze the winding and its insulation system at HF of CM signals, the basic lumped parameter equivalent circuit of a phase winding at HF should be observed as in Fig. 4 [25-27]. Here: L is the total inductance and it includes main and leakage inductances, R is the serial connection of ac winding resistance and core resistance, C represents stray capacitance which consists of turn-to-turn and turn-to-ground capacitances, which will be further elaborated on in Section 4. Inductance and resistance are frequency dependent, due to eddy-currents in the core, and skin and proximity effect in the winding. Stray capacitance is assumed not to be frequency dependent [29].

In a more detailed representation, equivalent circuits of a coil are given in Figs. 5 and 6 [30] and [32]. Some authors are applying the same equivalent circuits to represent the winding [31]. These equivalent circuits represent a coil and designations are: R_{Pl} represents AC iron losses (eddy-current and hysteresis losses inside the magnetic core and the frame); R_{Cl} represents dissipative phenomena due to HF capacitive current and dielectric losses; R_{L1} is AC wire resistance; C_1 represents turn-to-turn capacitance; L_1 is overall inductance of the coil (sum of overhang part and slot part of the coil). Overall inductance L_1 and AC wire resistance are frequency dependent, but in order to use this equivalent circuit in frequency and time domain, these values are usually set to average value [11]. Values of R_{Pl}, R_{Cl} and R_{L1} are usually a couple of kΩ÷10x kΩ, 10x Ω and 100x Ω, respectively. Additional capacitance towards the ground must be taken into consideration with the resistance R_g and the capacitance C_g.

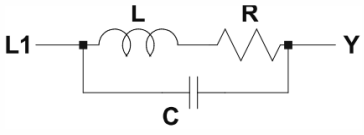

Fig. 4: The basic lumped parameter equivalent circuit of a phase winding in HF domain

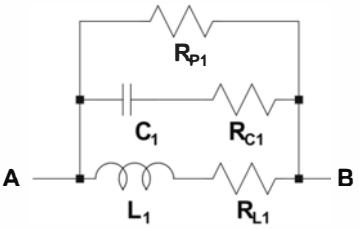

Fig. 5: Detailed equivalent circuit of a coil at HF

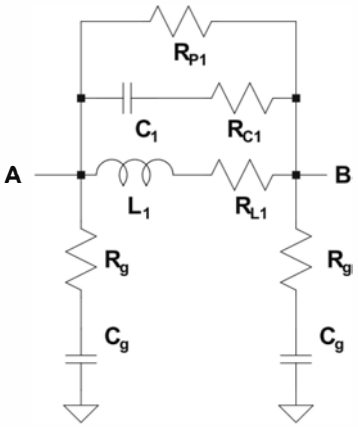

Fig. 6: Detailed equivalent circuit of coil at HF with capacitance towards the ground being taken into consideration

IV. TYPES OF CAPACITANCES

Basic types of parasitic capacitances regarding the windings are turn-to-turn and turn-to-ground. Additionally, coil-to-coil, coil-to-ground, phase-to-phase, and phase-to-ground capacitances can be observed as an extension of basic types [47].

From the two basic types of capacitances, the capacitance matrix [48, 49] can be formed with diagonal elements C_{ii}, which are called "self-capacitance coefficients" [49-55]. They are positive constants and represent, the sum of capacitances between the i^{th} conductor and every other (j^{th}) conductor in the system, as well as between the i^{th} conductor and its ground. Non-diagonal elements C_{ij}, which are called "mutual-capacitance coefficients", and exist between the i^{th} and j^{th} conductor. They are negative constants that represent the mutual partial capacitance between the i^{th} and j^{th} conductor in the system. In Fig. 7, an example of a random coil cross-section with four conductors is given.

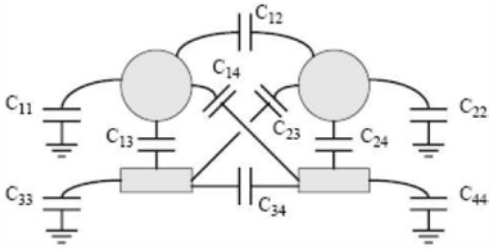

Fig. 7: An example of capacitances between four conductors of which two have round and two have rectangular cross-section [54]

The combination of cross-sections of the conductors (two rectangular and two round conductors) is given deliberately. The capacitance matrix for this example is given with (1). For the general case, this matrix would be given with (2).

$$\begin{bmatrix} C_{11}+C_{12}+ \\ +C_{13}+C_{14} & -C_{12} & -C_{13} & -C_{14} \\ -C_{21} & C_{21}+C_{22}+ \\ +C_{23}+C_{24} & -C_{23} & -C_{24} \\ -C_{31} & -C_{32} & C_{31}+C_{32}+ \\ +C_{33}+C_{34} & -C_{34} \\ -C_{41} & -C_{42} & -C_{43} & C_{41}+C_{42}+ \\ +C_{43}+C_{44} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} C_{11}+C_{12}+ \\ +\cdots+C_{1n} & -C_{12} & \cdots & -C_{1n} \\ -C_{21} & C_{21}+C_{22}+ \\ +\cdots+C_{2n} & \cdots & -C_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ -C_{n1} & -C_{n2} & \cdots & C_{n1}+C_{n2}+ \\ +\cdots+C_{nn} \end{bmatrix} \quad (2)$$

A. Turn-to-Turn Capacitance

Turn-to-turn capacitance implies the capacitance between any two conductors inside the same coil. Turn-to-turn capacitance C_{tt} is calculated between the turns i and j ($i \neq j$). This capacitance can be calculated in different ways, depending on the shape of the conductor and their arrangement in the slot.

1) Formed winding – Conductors with rectangular cross-section: For rectangular conductors it is relatively easy to calculate C_{tt}. Thanks to the surface contours of form-wound coils, which are sufficiently and necessarily regular to permit the representation of a coil in a slot or end region by equivalent parallel-plate capacitors [33]. In this case, capacitance is given with (3), where ε, A, and d_e, are permittivity, conductor surface and distance between two turns edges, respectively [34].

$$C_{tt} = \varepsilon \cdot \frac{A}{d_e} \quad (3)$$

Figs. 8-10 present turn-to-turn capacitance for simple, two-turn coil, and one-layer and two-layer multi-turn coils. In the case as in Fig. 10, turn-to-turn capacitance will be different due to different surfaces between two adjacent turns ($C_{tt1} \neq C_{tt2}$).

Taking into account parallel plate capacitor, another approach for calculation of turn-to-turn capacitance is given in [28] and with regard to the Fig. 11. It is based on the calculation of the capacitance between two infinite, straight, parallel conductors in homogenous medium (in this case it will be assumed air).

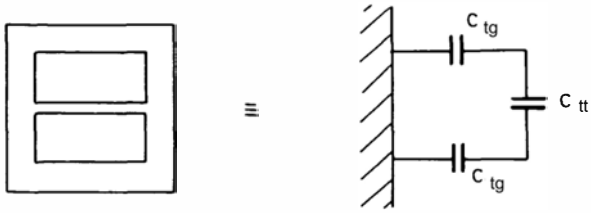

Fig. 8: Simple, two-turn coil and its capacitances [33]

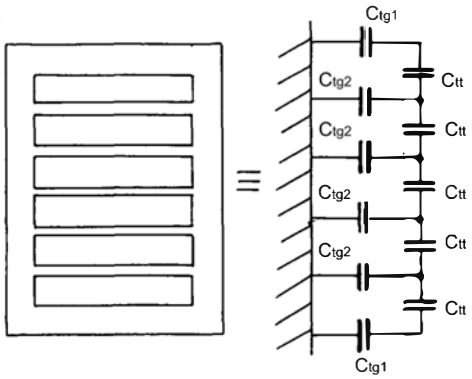

Fig. 9: Single-row coil and distributed network of its capacitances [33]

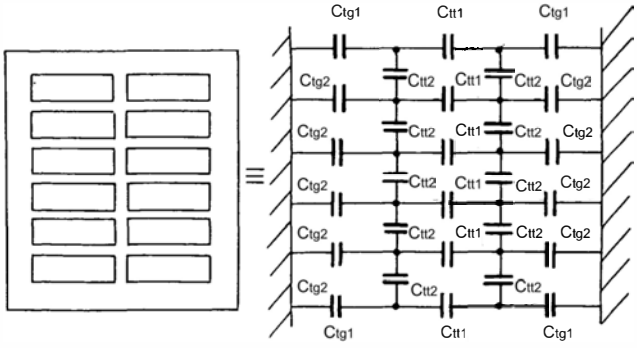

Fig. 10: Double-row coil and distributed network of its capacitances [33]

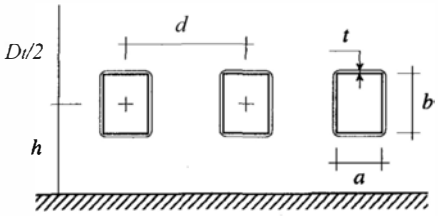

Fig. 11: Cross-section of rectangular wires and ground [28]

Turn-to-turn capacitance from Fig. 11 would be:

$$C_{tt} = \frac{k\,\varepsilon_o\,L\,b}{d-a} \tag{4}$$

The factor k includes edge effects which are the function of the winding geometry. Equation (4) does not consider insulation coating thickness, i.e. $t<<d-a$. If the insulation coating thickness cannot be neglected, the equation (5) should be used.

$$C_{tt} = \frac{k\,\varepsilon_o\,L\,b}{d-a-2\cdot t\cdot\left(1-\frac{1}{\varepsilon_r}\right)} \tag{5}$$

In equations (4) and (5) it is assumed that L is the turn length.

2) Formed winding – Conductors with round cross-section: In the case of two conductors with round cross-section in homogenous medium of permittivity ε, capacitance between them, according to [14] and [35], can be calculated as:

$$C_{tt} = \frac{\pi\,\varepsilon\,L}{\cosh^{-1}\left(\frac{d}{D}\right)} \tag{6}$$

Where L is the length of a conductor (turn), distance between centers of the two conductors is d, while D represents the diameter of these conductors. In the case of $d/D > 3$, mentioned capacitance reduces to:

$$C_{tt} = \frac{\pi\,\varepsilon\,L}{\ln\left(2\cdot\frac{d}{D}\right)} \tag{7}$$

In another approach, similar to the case of the rectangular wire from Fig. 11, capacitance between two turns can be calculated on the basis of the calculation of infinite, parallel conductors with round cross-section in homogenous medium as presented in Fig. 12 [28]. The calculation neglecting the insulation thickness is given by:

$$C_{tt} = \frac{\varepsilon_o\,\pi\,L}{\ln\left(\frac{d}{2\,r}+\sqrt{\left(\frac{d}{2\,r}\right)^2-1}\right)} \tag{8}$$

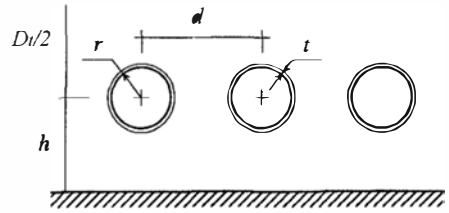

Fig. 12: Cross-section of round wires and ground, $D=2r$ [28]

Equation (8) is the same as (6) with regards to the mathematical identity between $\cosh^{-1}(x)$ and $\ln(x)$. If insulation thickness cannot be neglected, it should be taken into consideration by applying of the following equation:

$$C_{tt} = \frac{\varepsilon_o\,\pi\,L}{\ln\left(F+\sqrt{F^2-\left(1+\frac{t}{r}\right)^{\frac{2}{\varepsilon_r}}}\right)} \tag{9}$$

Where factor F is given by:

$$F = \frac{d/_{2\,r}}{\left(1-\frac{t}{r}\right)^{1-\frac{1}{\varepsilon_r}}} \tag{10}$$

Derivation of (9) is presented in detail in [28].

Main downside of the previous two methods described with equations (6)-(9) is the limitation to single-layer coils. Further, these two methods include only the capacitance calculated in regards to the shortest possible path along the center axis of two turns, i.e. axis which connects the centers of two observed turns (conservative approximation). The actual capacitance between two conductors will vary due to the roundness of the conductors, which means that the lines of the electric field will not have an equal length. In order to obtain a result which can be applied to a multi-layer coil, and to take into consideration different length paths between two conductors as given in Fig. 13, previous equations must be expanded.

The equivalent capacitance consists of three capacitances connected in series – capacitance of the insulation layer of the first turn, capacitance of the air gap between two turns, and capacitance of the second turn [36]. From Fig. 13 it can be seen that a basic cell for capacitance calculation can be extracted in regards to the symmetry as according to Fig. 14.

Further, from the geometrical symmetry of the coil and with the assumption that the turn in the middle is fully surrounded with other turns, a turn can be divided into elementary surfaces which face adjacent turn. The angle between two elementary cylindrical surfaces of adjacent turns covers $\pi/3$. Turns located at the edges of a coil differ

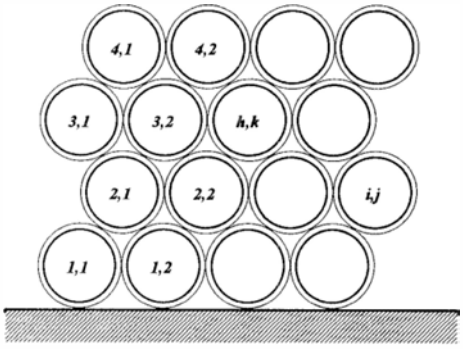

Fig. 13: Hexagonal arrangement of conductors in a multi-layer winding [36]

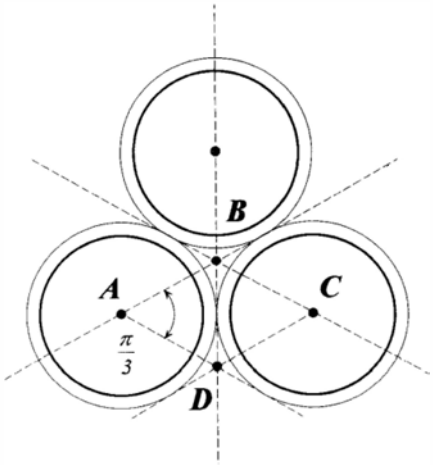

Fig. 14: A basic cell for the calculation of C_{tt} [36]

from this model, but in order to make a first-order approximation, all turns will be considered in accordance to this basic cell. This approximation is equal to neglecting the fringing effects. In the zone of π/3, the air gap path between two elementary cylindrical surfaces of adjacent turns is the length of a line of the electric field connecting the two opposite elementary cylindrical surfaces, i.e. x. This length is a function of angle θ, as shown in Fig. 15. In this region the capacitance must be integrated along the angle θ, i.e. over the angle of π/3. The elementary cylindrical surface for calculating the insulation layer capacitance is given in Fig. 16.

First, the capacitance of the insulating coating is calculated with respect to Fig. 16. The elementary capacitance of the cylindrical insulation coating shell is given by:

$$dC_c = \frac{\varepsilon_o\ \varepsilon_r}{dr} dl\ d\theta \tag{11}$$

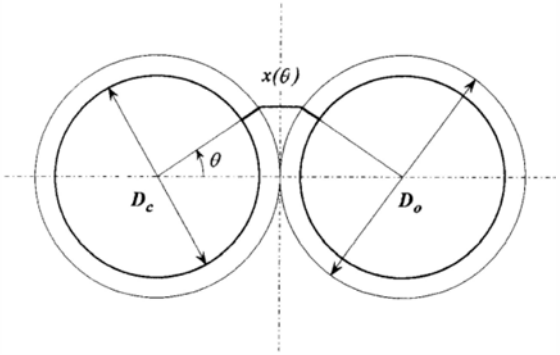

Fig. 15: Assumed path of an electric field line between two adjacent turns for calculating C_{tt} [36]

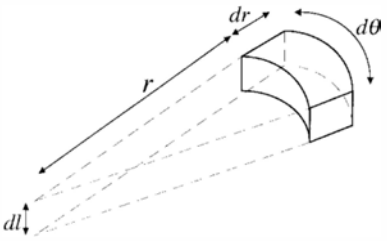

Fig. 16: The elementary cylindrical surface of an insulation coating [36]

The result of the equation (11) after the integration over the turn length L and insulation thickness t, will be:

$$dC_c = \frac{\varepsilon_o\ \varepsilon_r\ L}{\ln\frac{D_o}{D_c}} d\theta \tag{12}$$

The capacitance of the air gap is calculated considering the assumed paths as a function of θ. The paths are given by:

$$x(\theta) = D_o(1 - \cos\theta) \tag{13}$$

And the air gap capacitance is:

$$dC_g = \frac{\varepsilon_o\ L}{2(1 - \cos\theta)} d\theta \tag{14}$$

The total capacitance between two turns is:

$$dC_{tt} = \frac{dC_c\ dC_g}{dC_c + 2\ dC_g} \tag{15}$$

After the integration over the angle of π/3:

$$C_{tt} = \varepsilon_o L \frac{2\varepsilon_r \tan^{-1}\left[\frac{N \cdot M}{N \cdot \sqrt{\ln\left(\frac{D_o}{D_c} M\right)}}\right]}{\sqrt{2\varepsilon_r \ln\left(\frac{D_o}{D_c}\right) + \left(\ln\frac{D_o}{D_c}\right)^2}} \tag{16}$$

where:

$$M = -1 + \sqrt{3} \tag{17}$$

and

$$N = 2\varepsilon_r + \ln\frac{D_o}{D_c}. \tag{18}$$

In order to simplify equation (16), instead of θ, a new angle θ^* is introduced. It is the angle at which the serial connection of elementary capacitances of the insulation coatings is equal to the elementary capacitance of the air gap, i.e.:

$$\theta^* \Rightarrow \frac{dC_c}{2} = dC_g \tag{19}$$

The capacitance of the insulating coating is now:

$$C_c = \frac{2\,\varepsilon_o\,\varepsilon_r\,L\,\theta^*}{\ln\frac{D_o}{D_c}} \tag{20}$$

If it is assumed that the insulation coating thickness s is small comparing to the conductor diameter, cylindrical shell can be further approximated with parallel plate capacitor, so (20) becomes:

$$C_c = \frac{\varepsilon_o\,\varepsilon_r\,L\,D_a\,\theta^*}{t} \tag{21}$$

And the air gap capacitance will be:

$$C_g = \varepsilon_o\,L\left[\cot\left(\frac{\theta^*}{2}\right) - \cot\left(\frac{\pi}{12}\right)\right] \tag{22}$$

Where D_a represents average diameter of the insulation coating:

$$D_a = \frac{D_o + D_c}{2} \tag{23}$$

With a couple of simple mathematical operations between (12), (14) (19), (20) and (21), angle θ^* can be expressed as:

$$\theta^* = \cos^{-1}\left(1 - \frac{2\,t}{\varepsilon_r\,D_a}\right) \tag{24}$$

Finally, the overall turn-to turn capacitance will be:

$$C_{tt} = \varepsilon_o\,L\left[\frac{\varepsilon_r\,D_a\,\theta^*}{t} + \cot\left(\frac{\theta^*}{2}\right) - 3.732\right] \tag{25}$$

Previous analysis is given under the assumption of uniformly-wound single-wire coils.

Detailed derivation of (25) is presented in [37].

3) Random winding (mush-wound cois) – Conductors with round cross-section: Random-wound coils imply bundle of round wires inserted into the slot, neglecting the order of the wires [38, 39]. This type of winding is used in low-voltage machines (up to 1kV). Due to the randomly inserted wire, it can happen that the first turn can be next to the last one, and in that case the voltage difference between these two turns is the highest. Not knowing the actual wire distribution inside the slot, it is impossible to calculate the turn-to-turn capacitance based on the coil geometry. The turn-to-turn capacitance can be obtained only by measurements and then calculating the capacitance via resonant frequency and inductance matrix as explained in [29] and [32], or via stored energy as presented in [40, 41].

B. Turn-to-Ground Capacitance

Turn-to-ground capacitances (C_{tg}) is the capacitance between the turn and the slot wall. It is also referred as a turn self-capacitance. It is larger than turn-to-turn capacitance and it can also be calculated in different ways, depending on the wire type and its configuration in the slot.

1) Formed winding – Conductors with rectangular cross-section: From Figs. 8-10 it can be noticed that C_{tg} will be the same for two-turn coil, but it will be different in the case of multi-turn coils. The difference will appear between the outer turns (top and bottom) and the inner turns, which will have the capacitance C_{tg1} and C_{tg2}, respectively ($C_{tg1} \neq C_{tg2}$). This difference appears due to difference of surfaces which are facing the slot wall. It is obvious that $C_{tg1} > C_{tg2}$ considering that the outer turn has larger surface.

Turn-to-ground capacitance for the coil in Fig. 11 can be calculated in the similar way as C_{tt}. If the insulation coating thickness is negligible, i.e. $t << d_1 - a/2$, the result will be:

$$C_{tg} = \frac{k\,\varepsilon_o\,L\,b}{h - \frac{a}{2}} \tag{26}$$

If the insulation coating thickness cannot be neglected, C_{tg} will be:

$$C_{tg} = \frac{k\,\varepsilon_o\,L\,b}{h - \frac{a}{2} - t\left(1 - \frac{1}{\varepsilon_r}\right)} \tag{27}$$

2) Formed winding – Conductors with round cross-section: For the case from Fig. 12, C_{tg} will be given by (28) if the insulation coating thickness can be neglected, i.e. $t << h\text{-}r$, if that is not the case, then expression (29) is applied.

$$C_{tg} = \frac{2\,\pi\,\varepsilon_o\,L}{\ln\left(\frac{h}{r} + \sqrt{\left(\frac{h}{r}\right)^2 - 1}\right)} \tag{28}$$

$$C_{tg} = \frac{2\,\pi\,\varepsilon_o\,L}{\ln\left(F' + \sqrt{F'^2 - \left(1 + \frac{t}{r}\right)^{\frac{2}{\varepsilon_r}}}\right)} \tag{29}$$

Where factor F' is given by:

$$F' = \frac{h/r}{\left(1-\frac{t}{r}\right)^{1-\frac{1}{\varepsilon_r}}} \tag{30}$$

To calculate turn-to-ground capacitance for a multi-layer coil from Fig. 13, similar methodology will be applied as for C_{tt}. If it would be assumed that the slot wall is the symmetry plane from Fig. 15, the path lengths of the electric field lines between the turn and the slot wall will be a half of the path lengths between two turns. This means that C_{tg} will be a serial connection of the coating capacitance given by (12) and a half of the air capacitance given by (14), as shown in Fig. 17. After solving a simple network of serial capacitances it can be obtained that C_{tg} is double the C_{tt} given by (25), i.e.:

$$C_{tg} = 2\,C_{tt} \tag{31}$$

In the reality, the basic cell for calculating C_{tg} is wider than the one used for calculating C_{tt}. The angle between the elementary cylindrical surfaces from Fig. 15 and the ground plane will actually be π/2. For the simplicity reasons, expression (31) is given as a first-order approximation.

3) Random winding (mush-wound cois) – Conductors with round cross-section: As explained in the case of C_{tt}, for random-wound coil it is not possible to determine C_{tg} on the basis of coil geometry. In [42] C_{tg} was determined as an average value of the measured coil-to-ground capacitances, divided with the number of turns. It can be stated that turn-to-ground capacitance can be obtained only by measurements [32] and [42].

C. Layer-to-Layer and Layer-to-Ground

In the previous interpretation of turn-to-turn and turn-to-ground capacitance it was explained how to calculate mentioned capacitance, considering them as an elementary capacitances regarding the windings in EM. The next step would be to consider layer-to-layer C_{ll} and layer-to-ground C_{lg} capacitances. As above-mentioned, coils, i.e. windings can be single- or multi-layer. For a single-layer coil (winding) C_{ll} does not exist, while C_{lg} can be observed through the equivalent Π circuit as in [27] by solving the network of distributed capacitances by applying D-Y transformation for capacitances. In the case of multi-layer coils, C_{ll} and C_{lg} can be calculated according to [43], which suggests to observe a layer as plate:

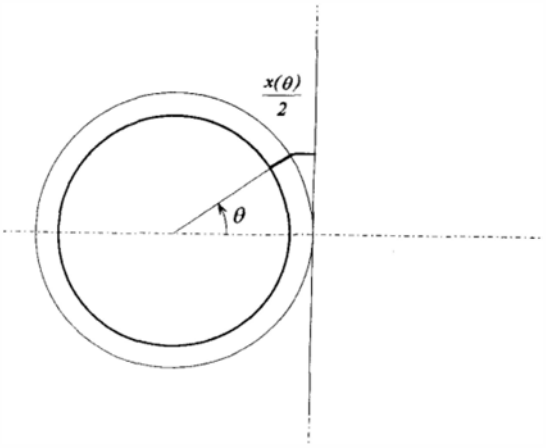

Fig. 17: Assumed path of the electric field line between two adjacent turns for calculating C_{tg} [36]

$$C_{lx} = \frac{b_w\, l}{S_e} \tag{32}$$

Where x in the subscript stands for l – layer or g – ground. In the expression b_w, l and S_e represent coil width, an average length of a turn, and the distance between horizontal axis of a layer, respectively. For C_{ll}, S_e is calculated as:

$$S_e = \Delta_{ll} + 1.26\,D_o - 1.15\,D_c \tag{33}$$

While for C_{lg}, S_e is:

$$S_e = \Delta_{lg} + \frac{1}{2}(1.26\,D_o - 1.15\,D_c) \tag{34}$$

Distance between two layers, i.e. between a layer and ground is given with Δ_{ll}, i.e. Δ_{lg}.

Alternative expression for calculating C_{ll} is presented in [44]:

$$C_{ll} = \frac{n_t\,(n_t+1)\,(2\,n_t+1)}{6\,n_t^2}\; l\; C_{tt} \tag{35}$$

where n_t is number of turns in the layer and l is average length of a turn.

Voltage distribution among layers must be taken into consideration as well, as shown in [43, 44].

If z represents the number of layers in a coil then self-capacitance of a coil is given as:

$$C_{cs} = C_{ll}\,(z-1)\left(\frac{2}{z}\right)^2 \tag{36}$$

D. Coil-to-Coil and Coil-to-Ground

Depending on the form of a coil (rectangular or round), coil-to-coil capacitance C_{cc} and coil-to-ground C_{cg} can be approximated with the expressions for a parallel plate capacitor or round conductor [43-45].

E. Phase-to-Phase and Phase-to-Ground

The phase-to-phase capacitances C_{pp} are formed mainly by the winding parts of the different phases U, V and W, in the winding overhang and inside the slots [21]. This type of capacitance is usually an order of magnitude smaller than phase-to-ground capacitance [21] and [31]. This difference is attributed to the different parts of a

machine that form the capacitances. The stator windings are embedded into the stator slots of the stator core iron stack where the area of contact is large and the distance is small when compared with the area and the distance between the phases in the winding overhang.

The stator phase-to-ground capacitance C_{pg} can be approximated as a $Q_s/3$ parallel plate capacitor, where Q_s is a number of stator slots [21] and [46].

V. Discussion and Recommendations

Many assumptions and approximations are applied in order to simplify the calculations of a winding parasitic capacitive couplings. Further, the comparison of results obtained by analytical methods and measurements done in referenced publications report a deviation of 20% [21-37] up to even 174% [21]. Thus, authors of mentioned publications are proposing correction coefficients.

The authors of this article would suggest following recommendations to be taken in account when determining the parasitic capacitances in EM:

- details of design of EM should be known before proceeding with the parasitic capacitance calculation. These details imply the knowledge of the complete insulation system applied, number and shape of the wire used, the number of slots and their shape, etc.
- capacitances between non-adjacent turns, and between non-adjacent layers should not be neglected.
- finite elements (FE) based calculations in combination with analytical analysis presented in this paper, should be used in order to determine parasitic capacitances with increased accuracy.
- measurements on EMs should be done without the rotor in place, in order to avoid stator winding-to-rotor capacitance and bearing capacitance – in that way only turn-to-turn capacitance and turn-to-ground capacitance are considered.
- voltage distribution along the coil must be considered when designing a coil. In order to minimize the capacitance, layers in a coil should be wound in the same direction. This, however demands longer connection between adjacent layers, thus it presents a trade-off between more active material for the coil production and minimizing the capacitances.
- dynamic effects, such as the influence of proximity effects that can lead to inductance variations within the coil should be considered.

VI. Conclusion

Various analytical methods for the calculation of the parasitic capacitive couplings in regards to a winding are presented in this paper. As such, many simplifications have been applied in order to obtain the presented equations. However, it can be concluded that truly accurate results can only be obtained by applying accurate analytical or FE based calculations and considering the real configuration of the winding in parallel with measurements. Future work will be focused on deriving the complete parasitic capacitance matrix based on analytical and FE models in order to implement improved HF model in EMs. Such improved model can then be used during the EM design process in order to minimize the effects of EMI.

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